In the Claims

Cancel claims 1-4, 16, 17 and 37-49 without prejudice.

5. A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

6. The method of claim 5, wherein said three devices comprise peripheral circuitry.

7. The method of claim 5, wherein said three devices comprise NMOS field effect transistors.

8. The method of claim 5, wherein said three devices comprise NMOS field effect transistors comprising peripheral circuitry.

9. The method of claim 5, wherein the three devices comprise PMOS field effect transistors.

10. The method of claim 5, wherein said three devices comprise PMOS field effect transistors comprising peripheral circuitry.

11. The method of claim 5, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

12. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

13. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

14. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

15. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

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50. A semiconductor processing method comprising implanting dopant through one common mask, implanting comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, the one common mask masking only portions of some of the devices which receive the halo implant, the devices receiving the halo implant comprising MOS field effect transistors having source regions and drain regions and the mask comprises a mask masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

51. The method of claim 50, wherein the three devices comprise peripheral circuitry.

52. The method of claim 50, wherein the three devices comprise memory circuitry.

53. The method of claim 50, wherein the three devices comprise NMOS field effect transistors.

54. The method of claim 50, wherein the three devices comprise NMOS field effect transistors comprising peripheral circuitry.

55. The method of claim 50, wherein the three devices comprise PMOS field effect transistors.

56. The method of claim 50, wherein the three devices comprise PMOS field effect transistors comprising peripheral circuitry.

57. The method of claim 50, further comprising, prior to implanting, a common masking act comprising masking only portions of some peripheral circuitry devices which receive the halo implant.

58. The method of claim 50, further comprising, prior to implanting, a common masking act comprising masking only portions of some of the devices which receive the halo implant, wherein the devices which receive the halo implant comprise NMOS field effect transistors and wherein the portions comprise portions of peripheral circuitry devices.

59. The method of claim 50, further comprising, prior to implanting, a common masking act comprising masking only portions of some of the devices which receive the halo implant, wherein the devices which receive the halo implant comprise PMOS field effect transistors and the portions comprise portions of peripheral circuitry devices.

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60. The method of claim 50, further comprising, prior to implanting, a common masking act comprising masking only portions of some of the devices which receive the halo implant, wherein the devices which receive the halo implant comprise NMOS field effect transistors and the portions comprise portions of peripheral and memory circuitry devices.